Description:

Coordinate between input data (num\_of\_signals\_g) to output data (data\_width\_g) when input > output. We save at first the incoming data (when it is valid) and start to output it in the width of out\_width\_g every clock cycle. In the case that the last output is smaller than that width, we add 0 to the MSB until it's fit, in order to not change the number value.

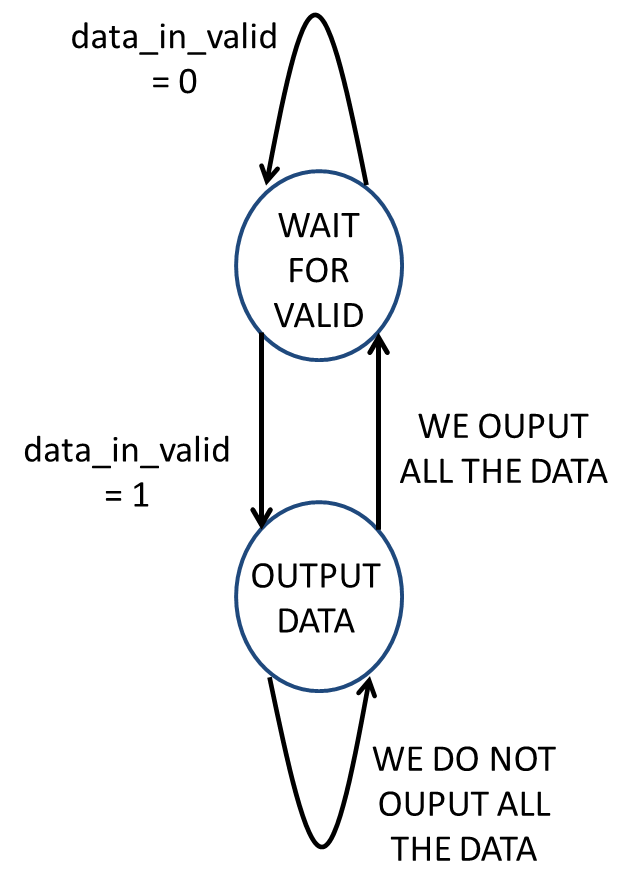
Generic table

|  |  |  |
| --- | --- | --- |
| Name | Width | Description |
| reset\_polarity\_g | 1 | '1' reset active high, '0' active low |
| out\_width\_g | 3 | Width of outputting data |
| in\_width\_g | 8 | Width of incoming data |

Signals table

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Direction | Width | Description |
| clk | In | 1 | System clock |
| Reset | In | 1 | System reset |
| data\_in | In | in\_width\_g | Incoming data |
| data\_in\_valid | In | 1 | Incoming data valid |
| data\_out | In | out\_width\_g | Outputting data |
| data\_out\_valid | In | 1 | Outputting data valid |

IN BIG OUT CORDINATOR FSM



Output table

